Assignee: Intel Corporation
Docket No.: 2207/10377

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(S)	:	Jeffrey F. Harness, et al.
SERIAL NO.	:	09/750,090
FILED	:	December 29, 2000
FOR	:	Digital Low Pass Filter
GROUP ART UNIT	:	2124
EXAMINER	:	Chat C. Do

M/S: APPEAL BRIEF - PATENT
COMMISSIONER FOR PATENTS
P.O. Box 1450
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ATTENTION: Board of Patent Appeals and Interferences

APPEAL BRIEF UNDER 37 CFR 41.37

Dear Sir:

This brief is in furtherance of the Notice of Appeal, and the Notification of Non-Compliant Appeal Brief date July 26, 2007.

1. REAL PARTY IN INTEREST

Intel Corporation is the real party in interest for all issues related to this application.

2. RELATED APPEALS AND INTERFERENCES

There are no other appeals, interferences, or judicial proceedings known to Appellant or Appellant's legal representative, which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

3. STATUS OF THE CLAIMS

This application currently contains claims 1-25. Claims 2-6, 11-18 and 20-25 have been allowed. Claims 1, 7, 10, and 19 were rejected under 35 U.S.C. § 102(b) as being anticipated U.S. Patent No. 5,034,744 to Obinata ("Obinata"). Claims 8-9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Obinata. Claims 1, 7-10, and 19 are the claims on appeal.

4. STATUS OF AMENDMENTS

There are no currently outstanding amendments. The attached listing of claims (section 8), reflects the status of the claims including this amendment.

5. SUMMARY OF THE INVENTION

In the embodiment of claim 1, a method is provided for filtering over-sampled data. In a first operation, a word of over-sampled data is received that includes a plurality of sample bits

for each of a plurality of data bits (see, e.g., pg., 3, line 24 to pg. 4, line 7 and Fig. 2a). In a second operation, a sample bit is detected having one logic value and adjacent bits on both sides of said sample bit each having an opposite logic value to the one logic value of the sample bit (see, e.g., pg. 5, lines 18-21). In a third operation, the received word is output with the sample bit having the one logic value inverted (see, e.g., pg. 6, lines 9-14 and Fig. 2b).

In the embodiment of claim 10, an apparatus is provided for filtering over-sampled data. The apparatus includes detection logic coupled to receive a word of over-sampled data including a plurality of sample bits for each of a plurality of data bits and to detect a sample bit having one logic value and adjacent bits on both sides of said sample bit each having an opposite logic value to the one logic value of said sample bit (see, e.g., pg. 3, line 24 to pg. 4, line 7 and pg. 5, lines 18-21; and element 17 of Fig. 1 and element 41 of Fig. 4). The apparatus also includes an output circuit outputting the received word with the sample bit having said one logic value inverted (see, e.g., pg. 6, lines 9-14 and element 44 of Fig. 4).

In the embodiment of claim 19, a computer readable memory is provided containing program instructions that, when executed by a processor, cause the processor to perform a number of operations. In a first operation, a word of over-sampled data is received that includes a plurality of sample bits for each of a plurality of data bits (see, e.g., pg., 3, line 24 to pg. 4, line 7 and Fig. 2a). In a second operation, a sample bit is detected having one logic value and adjacent bits on both sides of said sample bit each having an opposite logic value to the one logic value of the sample bit (see, e.g., pg. 5, lines 18-21). In a third operation, the received word is output with the sample bit having the one logic value inverted (see, e.g., pg. 6, lines 9-14 and Fig. 2b).

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. The rejection of claims 1, 7, 10, and 19 under 35 U.S.C. § 102(b) as being anticipated U.S. Patent No. 5,034,744 to Obinata ("Obinata").

B. The rejection of claims 8-9 under 35 U.S.C. § 103(a) as being unpatentable over Obinata.

7. ARGUMENT

Under 35 U.S.C. §102(b), a claim is invalid if the invention claimed therein is described in a patent issuing more than one year prior to the filing of the subject patent application. Though a patent reference may have issued early enough (or filed early enough as the case for 35 U.S.C. §102(e)), that reference must also enable one skilled in the art to practice the claimed invention. *See* Akzo N.V. v. U.S. Int'l Trade Comm'n, 1 U.S.P.Q.2d (BNA) 1241, 1245 (Fed. Cir. 1986).

Absent anticipation it may be possible to combine two or more patents together to render a claimed invention obvious, and unpatentable, under 35 U.S.C. § 103(a). In determining whether the claims are unpatentable it is necessary to look to what the references actually teach. "It is impermissible within the framework of § 103 to pick and choose from any one reference only so much of it as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art." In Re Wesslau, 147 U.S.P.Q. (BNA) 391, 393 (C.C.P.A. 1965). Accordingly, a prior art reference must be considered in its entirety, and portions thereof must be taken in proper context. MPEP §

2141.02; Bausch & Lomb, Inc. v. Barnes-Hind, Inc., 230 U.S.P.Q. (BNA) 416, 419 (Fed. Cir. 1986).

Claims 1, 10 and 19

Claim 1 recites "detecting a sample bit having one logic value and adjacent bits on both sides of said sample bit each having an opposite logic value to the one logic value of said sample bit" and "outputting the received word with the sample bit having said one logic value inverted." Independent claims 10 and 19 have similar limitations.

Obinata does not teach or suggest these features. The Office Action cites Col. 2, lines 46-62 and the Abstract of Obinata as support for teaching the detecting and outputting operations of claim 1. Col. 2, lines 48-55 states that "a detecting circuit" is provided "for detecting status changes that results in generation of glitches in digital data to be inputted into the DAC, a pulse generating circuit for generating deglitching pulses for suppressing the glitches in response to outputs of the detecting circuit, and an operation circuit for cancelling glitches included in converted outputs of the DAC." The language of the Abstract is similar.

Though Obinata discusses the detection of "status changes," Obinata does not teach or suggest detecting a sample bit having one logic value and adjacent bits on both sides of the sample bit having an opposite logic value. Looking at Fig. 1, serial data is provided by oversampling digital filter 20 to S/P converting circuit 23. Circuit 23 outputs 16-bit parallel values as bits O_1 to O_{16}. Values O_1 to O_4 are provided to D-type flip-flops 30-33. Looking at Fig. 1, and Col. 4, lines 47-57, it is clear that a comparison is made between a sample bit (i.e., the input into one of the D-type flip-flops) and the previous sample bit (i.e., the output of the same

D-type flip-flop). Looking at D flip-flop 33, the comparison is made by XOR gate 37. If both inputs to this gate are the same, then the output will be a logic "0." If both inputs to this gate are different (indicating a glitch), then the output will be a logic "1" (or "H" as stated in Obinata). The outputs of the XOR gates 34-37 are used to make a correction of a particular type of glitch with the Philips TDA15431S1 DAC as explained in more detail at Col. 3, lines 14-45. The eventual outputs of NAND gates 46 and 47 are used in the analog circuits 27 and 28.

Though Obinata discusses the detection of "status changes," it is clear from the specification in Obinata, that such a "status change" is the situation where a previously sampled bit is different from a current sampled bit. There is no disclosure in Obinata, and the circuit of Fig. 1 does not support, detecting whether a sample bit has one logic value while adjacent **bits** on both sides of the sample bit have opposite logic values.

In the Response to Arguments section of the Final Office Action, the Examiner states that "the current claim language does not define or require any particular structure or component for detecting the sample bit having one logic value and adjacent bits on both sides of [the] sample bit having one logic value and adjacent bits on both sides of [the] sample bit each having an opposite logic value to the one logic value of [the] sample bit. Therefore, any reference discloses a method of detecting and suppression [of] a single bit as glitch, that reference would either inherently or expressively disclose the step of detecting a sample bit having one logic value and adjacent bits on both sides of [the] sample bit each having an opposite logic value to the one logic value of [the] sample bit. Without detecting the both [sides] of [the] glitch, there is no way of telling whether the bit is a glitch or a correct bit. In addition, the reference clearly discloses that after a glitch is detected, it will be deglitched accordingly (e.g., col. 2, lines 36-63)."

The cited section of Obinata is the Summary of the Invention section and includes "objects of the invention." The Summary refers to the circuit described in the Detailed Description section of the patent. The claim language of the independent claims refers to "detecting a sample bit having one logic value and adjacent bits on both sides of said sample bit each having an opposite logic value to the one logic value of said sample bit" and "outputting the received word with the sample bit having said one logic value inverted." (e.g., claim 1). If such language reads on any structure or component, then for a reference to be a proper reference under 35 U.S.C. § 102 it must teach such a detection, or such must be inherent from it. Neither is true with Obinata.

A glitch in Obinata is detected when a sample bit is different than the previous sample bit. There is no disclosure, inherent or otherwise for determining whether adjacent bits on both sides of a sample bit have an opposite logic value than that of the sample bit. Looking at Fig. 1, the comparison that is taking place at the output of the D-type flip-flops 30-33 is the comparison of the current bit (input to the flip flop) with the previous bit (output of the flip-flop). That is the explicit disclosure of the reference. There is nothing inherent in Obinata that even remotely suggests that both bits adjacent to the sample bit are being compared to the logic value of the sample bit.

The Office Action states that "without detecting the both side of glitch, there is no way of telling whether the bit is a glitch or a correct bit." That statement is not supported by the specification of Obinata. Col. 3, lines 14-57 describes the type of glitch that is the focus of the circuit of Fig. 1. As seen from Fig. 1, the indication of whether there is a difference between a current bit and a previous bit is shown by the outputs of XOR gates 34-37, the combinatorial logic to the right of the XOR gates. The output of NAND gate 39 becomes low only with the

second most significant bit changes value without the most significant bit changing its value (see Col. 3, lines 58-62). The other gates are making similar types of comparisons to provide a positive or negative deglitching pulse (see Col. 5, line 57 to Col. 6, line 2). See also Fig. 2a, which shows the comparison of eight bit values (i.e., the outputs of element 23 and the outputs of flip-flops 30-33).

The feature of independent claims 1, 10 and 19 is neither shown, explicitly or inherently, by Obinata and is not obvious in view of Obinata disclosure of correcting a particular type of glitch found in a Philips TDA 1541S1 DAC. Accordingly, reversal of the rejections of claims 1, 7-10 and 19 under 35 U.S.C. §§ 102(b) and 103(a) is respectfully requested.

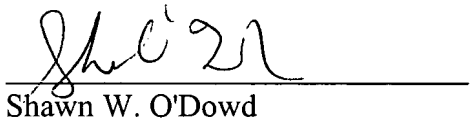
CONCLUSION

Appellants respectfully request that the Board of Patent Appeals and Interferences reverse the Examiner's decision rejecting claims 1, 7-10 and 25 under 35 U.S.C. §§ 102(b) and 103(a) direct the Examiner to pass the case to issue.

The Commissioner is hereby authorized to charge the appeal brief fee of $500.00 and any additional fees which may be necessary for consideration of this paper to Kenyon & Kenyon Deposit Account No. 11-0600. A copy of this sheet is enclosed for that purpose.

Respectfully submitted,

Date: November 26, 2007



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APPENDIX

(Brief of Appellants Jeffrey F. Harness et al.
U.S. Patent Application Serial No. 09/750,090)

8. CLAIMS ON APPEAL

The claims in their current form (including those claims under appeal) are presented below:

1. (Rejected) A method of filtering over-sampled data comprising:

a. receiving a word of over-sampled data including a plurality of sample bits for each of a plurality of data bits;

b. detecting a sample bit having one logic value and adjacent bits on both sides of said sample bit each having an opposite logic value to the one logic value of said sample bit; and

c. outputting the received word with the sample bit having said one logic value inverted.

2. (Allowed) A method of filtering over-sampled data comprising:

a. receiving a word of over-sampled data including a plurality of sample bits for each of a plurality of data bits;

b. detecting a sample bit having one logic value and, on either side of it, bits having an opposite logic value wherein said detecting comprises:

b1. exclusively ORing each sample bit in said word separately with each bit on either side of the sample bit; and

b2. ANDing the results of said exclusive ORing; and

c. outputting the received word with the sample bit having said one logic value inverted.

3. (Allowed) The method of claim 2 and further including providing a history bit to supply a bit to be exclusively ORed with the most significant bit of said word.

4. (Allowed) The method according to claim 3 wherein a plurality of words in succession are received, with the operations a, b, and c of claim 2 performed for each word, and further including saving the least significant bit of a last previous word received as the history bit for the next word received.

5. (Allowed) The method according to claim 4 comprising receiving words until the end of a packet is reached.

6. (Allowed) The method of claim 2 wherein said outputting comprises outputting each of said sample bits uninverted if the result of said ANDing is one logic level and inverted if the result is the other logic level.

7. (Rejected) The method according to claim 1 further comprising over-sampling said data and receiving said word from at least one over-sampler.

8. (Rejected) The method according to claim 7 and further comprising selecting a word to be received from between two over-samplers.

9. (Rejected) The method according to claim 1 wherein said over-sampled data is USB 2.0 data.

10. (Rejected) Apparatus for filtering over-sampled data comprising:

a. detection logic coupled to receive a word of over-sampled data including a plurality of sample bits for each of a plurality of data bits and to detect a sample bit having one logic value and adjacent bits on both sides of said sample bit each having an opposite logic value to the one logic value of said sample bit; and

b. an output circuit outputting the received word with the sample bit having said one logic value inverted.

11. (Allowed) Apparatus for filtering over-sampled data comprising:

a. detection logic coupled to receive a word of over-sampled data including a plurality of sample bits for each of a plurality of data bits and to detect a sample bit having one logic value and on either side of it, bits having an opposite logic value, said detection logic further comprises

a1. a plurality of terminals for receiving said sample bits for each of a plurality of data bits;

a2. a plurality of first two input logic circuits to perform an exclusive OR function, each having its inputs coupled to two adjacent terminals; and

a3. a plurality of second two input logic circuits to perform an AND function, each having as inputs outputs of two adjacent first logic circuits

b. an output circuit outputting the received word with the sample bit having said one logic value inverted.

12. (Allowed) The apparatus of claim 11 and further including a storage element to store a history bit, an output of said storage element coupled to one of said first logic circuits having as a second input a sample bit which is most significant.

13. (Allowed) The apparatus of claim 12 wherein said output circuit comprises:

a. a plurality of inverters, one coupled to each terminal; and

b. a plurality of multiplexers, each having a first data input coupled to an output of one of said inverters, an second data input coupled to the corresponding terminal, and a control input coupled to the output of the one of said second logic circuits associated with said terminal and an output.

14. (Allowed) The apparatus of claim 13 wherein a plurality of words in succession are to be received, said storage element having an input coupled to the least significant sample bit and having a clock input to clock said input to its output prior to receiving a new word.

15. (Allowed) The apparatus of claim 14 and further comprising an over-sampler to supply said words to said terminals.

16. (Allowed) The apparatus of claim 15 wherein two over-samplers are provided and further including a selection circuit to select between two over-samplers.

17. (Allowed) The apparatus of claim 16 wherein said selection circuit is a multiplexer.

18. (Allowed) The apparatus of claim 13 wherein said over-sampled data is USB 2.0.

19. (Rejected) A computer readable memory containing program instructions that, when executed by a processor, cause the processor to:

a. receive a word of over-sampled data including a plurality sample bits for each of a plurality of data bits;

b. detect a sample bit having one logic value and adjacent bits on both sides of said sample bit each having an opposite logic value to the one logic value of said sample bit; and

c. output the received word with the sample bit having said one logic value inverted.

20. (Allowed) A computer readable memory containing program instructions that, when executed by a processor, cause the processor to:

a. receive a word of over-sampled data including a plurality sample bits for each of a plurality of data bits;

b. detect a sample bit having one logic value and, on either side of it, bits having an opposite logic value

c. exclusively OR each sample bit in said word separately with each of the bits on either side of the sample bit; and

d. AND the results of said exclusive ORing; and

e. output the received word with the sample bit having said one logic value inverted.

21. (Allowed) A computer readable memory according to claim 20 wherein said processor is caused to provide a history bit to supply a bit for exclusive ORing with the most significant bit of said word.

22. (Allowed) A computer readable memory according to claim 21 wherein said processor is caused to receive a plurality of words in succession, with the operations a.-e. performed for each word and said processor is further caused to save the least significant bit of a last previous word received as the history bit for the next word received.

23. (Allowed) A computer readable memory according to claim 22 wherein said processor is caused to receive words until the end of a packet is reached.

24. (Allowed) A computer readable memory according to claim 23 wherein said processor is caused to output said each sample bits uninverted if the result of said ANDing is one logic level and inverted if the result is the other logic level.

25. (Allowed) A computer readable memory according to claim 21 wherein said over-sampled data is USB 2.0 data.

9. EVIDENCE APPENDIX

No further evidence has been submitted with this Appeal Brief.

10. RELATED PROCEEDINGS APPENDIX

Per Section 2 above, there are no related proceedings to the present Appeal.